CLAIMS

Having thus described our invention in detail, what we claim is new and desire to secure by the Letters Patent is:

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1. A DRAM cell array which comprises:

a plurality of memory cells which are arranged in rows and columns, each memory cell including a deep trench region having a vertical MOSFET and an underlying capacitor formed therein that are in electrical contact to each other through a buried-strap outdiffusion region which is present within a portion of a wall of each deep trench; and, each memory cell having a deep trench conductor forming an electrode of said underlying capacitor and an oxide collar formed in a portion of the deep trench;

collar oxide region formed on a remaining wall portion of the structure not containing said buried-strap outdiffusion region for electrically isolating a body contact from said underlying capacitor; and

trench top oxide (TTO) layer formed on a horizontal surface of the structure for isolating a deep trench conductor forming an electrode of said underlying capacitor and said buried strap from a gate conductor region;

underlying nitride layer formed between a top of said deep trench conductor and said buried strap region and underlying said formed TTO layer to eliminate possibility of TTO dielectric breakdown between said gate conductor and said capacitor electrode.

2. The DRAM cell array of Claim 1, wherein said TTO is formed on sidewalls and said horizontal surface, said memory cell being subject to a TTO oxide sidewall etch for removing said deposited TTO from said sidewall, wherein said underlying nitride layer is

additionally formed to line said sidewall regions to protect said collar oxide and prevent strap from being etched during said TTO oxide sidewall etch process.

3. The DRAM cell array of Claim 1, further including sacrificial oxide layer formed underneath said nitride layer formed to further eliminate possibility of TTO dielectric breakdown between the gate conductor and said deep trench conductor.

4. The DRAM cell array of Claim 1, wherein said nitride liner is deposited to a thickness ranging from 1.0 nm – 10.0 nm.

5. The DRAM cell array of Claim 1, wherein said vertical MOSFETs include gate dielectrics formed on inner surfaces of said walls of said memory cell.

6. A method of forming a DRAM cell array comprising the steps of:

(a) forming a plurality of deep trenches in an array portion of a Si-containing substrate having at least a hard mask formed thereon, said plurality of deep trenches being arranged in rows and columns and including at least collar oxide regions formed on walls thereof and a recessed deep trench conductor formed between said collar oxide regions and defining a capacitor electrode for a DRAM cell;

(b) forming a buried-strap outdiffusion region within a portion of said wall such that said portion partially encircles said wall;

(c) forming a nitride liner layer above a horizontal surface of said deep trench conductor and enclosing exposed sidewall and collar oxide regions;

(d) depositing top trench oxide (TTO) layer above said formed nitride liner layer;

(e) performing TTO sidewall etch to remove TTO oxide which has been deposited on the vertical sidewalls and collar oxide, said nitride liner acting to protect said collar oxide layer from being etched;

SUB B1

(f) performing nitride liner etch to remove the portion of the TTO nitride liner which is exposed after TTO oxide removal;

(g) forming a vertical MOSFET by growing a gate dielectric on exposed walls of said deep trenches and forming a gate conductor above said TTO oxide layer within the walls of the deep trenches lined with said gate dielectric, wherein said formed TTO layer having underlying nitride liner eliminates possibility of TTO dielectric breakdown between said gate conductor and said capacitor electrode of a DRAM cell.

7. The method of Claim 6, wherein prior to said step (c), the step of depositing sacrificial oxide layer above a horizontal surface of said deep trench conductor and surrounding exposed sidewall and collar oxide regions.

8. The method of Claim 6, wherein said nitride etch of step f) is selective to oxide and silicon.

9. The method of Claim 7, wherein said nitride etch of step f) is selective to said sacrificial oxide when said sacrificial oxide layer is grown under the nitride liner.

10. The method of Claim 6, wherein said collar oxide regions are formed by a local oxidation of silicon process.

11. The method of Claim 10, wherein prior to forming said collar oxide regions a capacitor is formed in a bottom portion of said deep trenches.

12. The method of Claim 11, wherein said capacitor is formed by the steps of: forming a buried plate diffusion region about said deep trenches, lining walls of said deep trenches with a node dielectric and filling said deep trenches with said deep trench conductor.

13. The method of Claim 11, wherein said recessed deep trench conductor is formed by deposition of a deep trench conductor and etching.

14. The method of Claim 6, wherein said buried-strap outdiffusion region is formed by a one-sided strap process.

15. The method of Claim 14, wherein said one-sided strap process includes forming a divot filled collar oxide region.